



**UNITED STATES DEPARTMENT OF COMMERCE**  
**Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

09/593,765 06/14/00 OHTANI

H 0756-2149

022204  
NIXON PEABODY, LLP  
8180 GREENSBORO DRIVE  
SUITE 800  
MCLEAN VA 22102

MMC2/0813

EXAMINER

NGUYEN, C

ART UNIT

PAPER NUMBER

2811

DATE MAILED:

08/13/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

# Office Action Summary

Application No.

09/593,765

Applicant(s)

OHTANI et al.

Examiner

CUONG Q NGUYEN

Group Art Unit

2811

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

## Status

- ☐ Responsive to communication(s) filed on \_\_\_\_\_
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- ☒ Claim(s) 1-47 is/are pending in the application.
- ☐ Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- ☒ Claim(s) 1-47 is/are rejected.
- ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- ☐ Claim(s) \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been received.
- ☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_
- ☐ received in this national stage application from the International Bureau (PCT Rule 1.7.2(a)).

\*Certified copies not received: \_\_\_\_\_

## Attachment(s)

- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2, 3
- ☒ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Interview Summary, PTO-413
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Other \_\_\_\_\_

Office Action Summary

Art Unit: 2811

## **DETAILED ACTION**

### ***Oath/Declaration***

1. The oath/declaration filed on 01/02/98 is acceptable.

---

### ***Information Disclosure Statement***

2. The Information Disclosure Statement filed on 06-14-00, 07-24-00 and 09-07-00 have been considered.

### ***Specification***

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
4. A new abstract is required that is clearly indicative of the invention to which the claims are directed. Note that, the claims are directed to semiconductor device not a method of making a semiconductor device.

### ***Claim Rejections - 35 U.S.C. § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 4, 6, 7, 8, 9, 11, 13, 14, 15, 16, 18, 20, 21, 22, 23, 24, 26, 28, 29, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang et al. (US 5,424,244).

Art Unit: 2811

Zhang et al. discloses a semiconductor device comprising: a semiconductor layer (204, a crystal silicon layer) formed on a surface of an insulating layer (203), the semiconductor including a first impurity region (208), a second impurity region (209), and a channel region in therebetween; a gate insulating film (205) formed on the semiconductor layer; a gate electrode (206) formed on the gate insulating film; a first insulating film (209) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; a second insulating film (210, a polyimide organic resin layer) formed on the first insulating film; an electrode (213) formed on the second insulating film and connected to the second impurity region (209); a transparent pixel electrode (211, an ITO layer) formed on the second insulating film, wherein the pixel electrode electrically connected to the electrode and is located under the electrode. See Zhang et al.'s Fig.11.

***Claim Rejections - 35 U.S.C. § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2811

Claims 1-4, 6-11, 13-18, 20-26, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hsieh (US 5,153,142) in view of Tran et al. (US 5,273,910).

Hsieh discloses a semiconductor device comprising: a doped polysilicon layer (14) formed on a surface of an insulating layer (12), the polysilicon layer including source/drain regions, and a channel region in therebetween; a gate insulating film (16) formed on the polysilicon layer; a gate electrode (18) formed on the gate insulating film; a first insulating film (20, a silicon oxide layer) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; an electrode (32, an aluminum layer) formed on the second insulating film and connected to one of source/drain regions; a transparent pixel electrode (30, an ITO layer) formed on the second insulating film, wherein the pixel electrode electrically connected to the electrode and is located under the electrode. See Hsieh's Fig.8.

Hsieh does not teach that the layer (14) is a single crystal silicon layer which includes a first impurity region, a second impurity region, and a channel region in therebetween; a second insulating film of a polyimide organic resin layer formed between the electrode, pixel electrode and the first insulating film.

Tran discloses a semiconductor device comprising: a semiconductor layer (42) can be formed of a single crystal silicon or a polysilicon layer on a surface of an insulating layer (51), the semiconductor including a first impurity region (45), a second

Art Unit: 2811

impurity region (46), and a channel region in therebetween; a gate insulating film (43) formed on the semiconductor layer; a gate electrode (49) formed on the gate insulating film; a first insulating film (a planarization layer 53) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; the planarization layer is planarized by coating with a second insulating film (a coating layer of polyimide organic resin layer) formed on the first insulating film to planarize the first insulating film (53). See Tran's Fig.5b and col.10 lines 8-32 and col.9 lines 60-64.

It would have been obvious to one of ordinary skill in the art to form the layer (14) in Hsieh's device of a single crystal silicon layer instead of polysilicon layer as taught by Tran et al. because single crystal silicon and polysilicon are common materials for forming the channel region in the thin film transistor device and they are interchangeable. It also would have been obvious to one of ordinary skill in the art to coat the first insulating film (20) in Hsieh's device with a polyimide layer as taught by Tran in order to obtain a smooth planarization layer (see Tran's col.10, lines 8-32). One of ordinary skill would have been motivated to do so because it is easier to form other element such as metalization on top of a smooth planarization interlayer insulating film than an uneven surface interlayer insulating film as shown in Hsieh's device.

Claims 5, 12, 19, 17, and 31-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hsieh in view of Tran et al. and further in view of Liauh (US 5,027,185).

Art Unit: 2811

Hsieh and Tran teach all the limitations of claims 1-4, 6-11, 13-18, 20-26, and 28-30 as shown above. However, Hsieh and Liauh do not teach that the conductor comprises a second conductive film of TiN.

Regarding claims 5, 12, 19, 27, 31-35, Liauh discloses a semiconductor device having electrodes connected to source/drain regions (3) comprise a first conductive film (11, an Al layer) and a second conductive film (10, a TiN layer) between the first conductive film and source/drain regions. See Liauh's Fig.8.

It would have been obvious to one of ordinary skill in the art to form the electrode of double layer TiN/Al as taught by Liauh because TiN layer acts as a barrier layer to prevent the migration of Al layer into the silicon source /drain regions which causes the junction spiking. See Liauh's col.2, lines 44-49.

Regarding claims 36-41, as above the electrode is formed of a TiN layer under an Al layer, therefore it is inherent that the TiN is interposed between the pixel electrode and the Al layer.

Regarding claims 42-47, as shown in Hsieh's Fig.8, another electrode formed the same material as the electrode connected to another source/drain region.

### ***Conclusion***

**7. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be fax d to TC 2800 via the TC 2800 Fax cent r located in Crystal Plaza 4, room 4-C23. Th faxing of such**

Art Unit: 2811

**papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

8. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

CN

August 3, 2001

  
TOM THOMAS  
SUPERVISORY PATENT EXAMINER